

[METHOD OF FABRICATING A FLASH MEMORY CELL]

Abstract of Disclosure

A simplified flash memory fabrication process is disclosed. The method includes the following steps: 1) forming a stacked layer on a substrate in the channel region, and the stacked layer is a polysilicon layer and a sacrificial layer formed atop the polysilicon layer; 2) depositing a dielectric layer to cover the channel region and the bit line region; 3) performing an isotropic dry etching process to etch away a predetermined thickness of the dielectric layer to expose a portion of the sacrificial layer, and at the same time, dividing the dielectric layer into a first portion dielectric layer positioned atop the sacrificial layer and a second portion dielectric layer that is not connected with the first portion dielectric layer; and 4) completely removing the sacrificial layer and the first portion dielectric layer.

Figures

Figure 1: A line graph showing the relationship between the number of figures and the number of pages. The x-axis represents the number of figures (0 to 10) and the y-axis represents the number of pages (0 to 10). The data points are as follows:

Number of Figures	Number of Pages
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10